

REMARKS

Claims 2-21 are pending in the application.

Claims 2-21 have been rejected.

Claims 2-21 remain pending in this application.

Reconsideration of the claims is respectfully requested.

I. CLAIM REJECTION UNDER 35 U.S.C. §102

Claims 2-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,666,506 to *Hesson*, hereinafter “Hesson”. This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

The Applicant directs the Examiner’s attention to independent Claim 2, which recites unique and novel limitations, including those emphasized below:

A pipelined microprocessor capable of detecting an instruction that loads data from a first memory location that was previously stored to, wherein the instruction is detected *without requiring computation of an external memory address of said first memory location for the instruction*.

In rejecting the Claim 1 limitations regarding detecting an instruction without requiring computation of an external memory address of said first memory location for the instruction the Examiner cited Hesson. Specifically, the Examiner stated the following:

Hesson did not explicitly show the instruction is detected without requiring computation of an external memory address as claimed. However, Hesson taught the comparison of the virtual address (see col.4 lines 65-67). Examiner holds that virtual address is not external, and the comparison is not computation. Therefore, Hesson is without address computation. [Section 3, Office Action dated February 6, 2008]

For the purpose if clarity, the cited section of Hesson is reproduced below:

The store barrier cache 11 performs a comparison of the next instruction prefetch fetch buffer virtual address against the virtual instruction address field in each of its cache entries. (Col. 4, ll. 65-67, Hesson)

Examiner states “Hesson does not explicitly show the instruction is detected with requiring computation of an external memory address as claimed.” A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Since Hesson does not show the instruction is detected with requiring computation of an external memory address as claimed, Hesson cannot anticipate independent Claim 2.

In addition, Applicant respectfully disagrees with the assertion by the Examiner that the virtual address operations of Hesson are “comparison” and “not computation”. Applicant notes that

Hesson explicitly requires a computation during the comparison. Hesson uses this computation to generate an output. The output is discussed in the remainder of the paragraph cited by the examiner.

If a store barrier cache hit results from the next instruction prefetch buffer virtual address, then the store barrier cache hit control output is a logic one. If no match is found, then the store barrier cache hit control output is a logic zero. (Col. 5, ll. 9-14, Hesson)

Since Hesson is generating an output, it is performing a computation to create that output. Therefore, Hesson does not anticipate the claimed limitation of detecting an instruction “without requiring computation of an external memory address of said first memory location for the instruction.”

Independent Claims 12 and 20 recite limitations that are similar to those recited and discussed above in independent Claim 2. Applicant respectfully asserts that the unique and novel limitations recited in independent Claims 2, 12 and 20 are not disclosed, taught or suggested in Hesson. Accordingly, independent Claims 2, 12, and 20 are patentable over the cited prior art references.

Dependent Claims 3-11, 13-19, and 21 depend directly or indirectly from Independent Claims 2, 12, and 20. Accordingly, for at least the reasons established above, Applicant respectfully submits that Claims 3-11, 13-19, and 21 are not anticipated by the cited art of record.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the § 102 rejection with respect to these claims.

CONCLUSION

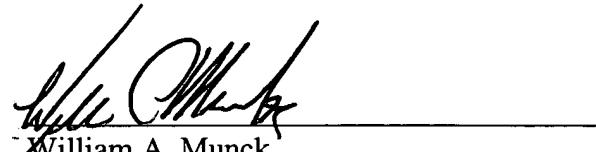
As a result of the foregoing, the Applicant asserts that the remaining claims in the Application are in condition for allowance, and respectfully requests that this Application be passed to issue.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at wmunck@munckbutrus.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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